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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/086,494	03/01/2002	Donald Charles Soltis JR.	10016692-1	2136

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EXAMINER	
ROSS, JOHN M	

ART UNIT	PAPER NUMBER
2188	5

DATE MAILED: 06/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/086,494	SOLTIS, DONALD CHARLES	
	Examiner	Art Unit	
	John M Ross	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 April 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17 and 19-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17 and 19-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 March 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Status of Claims

1. Claim 18 is canceled.

Claims 1-2, 10, 14 and 20 are amended.

Claims 1-17 and 19-26 are pending in the application.

Claims 1-17 and 19-26 are rejected.

Response to Amendment

2. Applicant's amendment filed on 6 April 2004 (Paper No. 4) in response to the office action mailed on 17 December 2003 necessitates new ground(s) of rejection under 35 U.S.C. 103 as presented below in this Office action.

Claim Objections

3. The amendment has overcome the objections to the claims.

Claim Rejections - 35 USC § 112

4. The amendment has overcome the rejections under 35 U.S.C. 112, paragraph 1.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-4, 6, 12-15, 20-21 and 23-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli (US 6,532,519) in view of Olukotun (Kunle Olukotun et al, "The Case for a Single-Chip Multiprocessor", Proceedings of the Seventh International Conference on Architectural Support for Programming Languages and Operating Systems, Cambridge, MA, Oct. 1996).

As in claims 1-4, 6 and 12-13, Arimilli discloses a system including a processor (Fig. 1, element 11a), a main memory (Fig. 1, element 18), a cache (Fig. 1, element 14a), and an interface between the processor and the cache (Fig. 1, element 20), where the cache is configured to receive data from an address of the main memory upon a request for the data by the processor (Column 1, lines 30-34), and the interface may be a crossbar (Column 2, lines 17-19).

Arimilli teaches a general method for interfacing a processor to a shared cache. It is readily apparent that this method is not limited to an L3 cache as in the embodiment of Arimilli, but may be applied to a shared cache at any level of the cache hierarchy.

Arimilli does not teach that cache is an on-chip cache located on the same die as the processor as required by claim 1.

Olukotun teaches a single-chip multiprocessor comprising a crossbar-connected shared L2 cache located on the same die as the processor (Fig. 3; § 4.2). Olukotun teaches that increasing integration density allows for higher clock rates, allowing microprocessor performance growth (§ 1, paragraph 1).

Regarding claim 1, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to integrate the cache and processor on the same die as taught by Olukotun, in the system of Arimilli, in order to allow for higher clock rates and performance growth as taught by Olukotun.

As in claim 2, Arimilli discloses the above system wherein the main memory is controlled by a memory controller (Fig. 1, element 17), and the crossbar interface is configured to link the memory controller, the processor and the cache (Fig. 1, element 20; column 2, lines 17-34).

As in claim 3, it is inherent in the teachings of Arimilli that when the processors and cache are connected by a crossbar switch as in claim 1 above, the connections to the crossbar are made through a plurality of ports (Fig. 1). Also as in claim 3 Arimilli teaches that a single address space may be partitioned among two or more caches such that a link between the

processor and cache would be made based upon the main memory address of a request for data by the processor (Column 1, lines 30-34; column 3, lines 51-67).

As in claim 4, Arimilli teaches that the processor is configured to associate a main memory address range (i.e. address space) with the cache (Column 1, lines 30-34; column 3, lines 51-67).

As in claim 6, Arimilli teaches that a main memory address range is mapped to the cache (Column 1, lines 30-34; column 3, lines 51-67).

It is noted in the rejections of claims 3-4 and 6 that mapping a main memory address range to a cache, and storing and retrieving data in the cache based upon a main memory address contained in a request from a processor, are well-known fundamental properties of any cache memory system such as that disclosed by Arimilli.

As in claim 12, it is axiomatic in the system of Arimilli that the crossbar interface comprises at least one crossbar (Column 2, lines 17-19).

As in claim 13, the system of Arimilli comprises a plurality of processors linked with the cache via the crossbar interface (Fig. 1, elements 11a – 11e; column 2, lines 17-24).

As in claims 14-15, Arimilli discloses a system comprising a plurality of processors (Fig. 1, elements 11a – 11e), a main memory (Fig. 1, element 18), a plurality of caches (Fig. 1, elements 14a – 14e), and an interface linking the caches and the processors (Fig. 1, element 20), where the cache is configured to receive data from a range of the main memory upon a request for the data by one of the processors (Column 1, lines 30-34), and the interface may be a crossbar (Column 2, lines 17-19).

Arimilli does not teach that caches are on-chip caches located on the same die as the plurality of processors as required by claim 14.

Olukotun is relied upon for the teachings relative to the rejection of claim 1 as above.

Regarding claim 14, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to integrate the caches and processors on the same die as taught by Olukotun, in the system of Arimilli, in order to allow for higher clock rates and performance growth as taught by Olukotun.

As in claim 15, Arimilli discloses that the processors may be configured to share at least one of the caches via the crossbar interface (Column 2, lines 38-43).

As in claim 20, Arimilli discloses a system configuration where

a plurality of main memory address ranges is mapped to a plurality of caches (Fig. 1, elements 14a – 14e and 18; column 1, lines 30-34; column 3, lines 51-67);

the caches are mapped to a plurality of processors (Fig. 1, elements 11a – 11e; column 2, lines 38-43); and

the processors and caches are linked using a crossbar interface (Fig. 1, element 20; column 2, lines 17-19).

Arimilli does not teach that the caches are on-chip, and providing the plurality of processors and plurality of caches on the same die as required by claim 20.

Olukotun is relied upon for the teachings relative to the rejection of claim 1 as above.

Regarding claim 20, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to integrate the caches and processors on the same die as taught by Olukotun, in the system of Arimilli, in order to allow for higher clock rates and performance growth as taught by Olukotun.

As in claim 21, Arimilli discloses that a processor is configured to interface with a cache (Column 2, lines 38-43), where also it is noted that mapping a main memory address range addressable by a processor to a cache is a well-known fundamental property of any cache memory system such as that disclosed by Arimilli.

As in claim 23, Arimilli discloses that a cache may be mapped to more than one processor (Column 2, lines 38-43).

As in claim 24, Arimilli discloses that two or more caches may be merged to act as a single larger cache (i.e. change the size of a cache) and that this association only requires programming a mode register and therefore does not require changing the crossbar interface (Column 2, line 49 to column 3, line 5; column 3, lines 44-67).

Claim 25 is rejected using the same rationale as for the rejection of claim 20, further noting that it is well known in the art that fabricating multiple components on the same die can improve speed and reduce power consumption, and therefore it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to configure the processing system of Arimilli and Olukotun on a single die in order to improve speed and reduce power consumption.

As in claim 26, Arimilli teaches that more than one cache may be mapped to one processor (Column 3, lines 51-58).

7. Claims 5, 7-10, 16-17 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli (US 6,532,519) in view of Olukotun (Kunle Olukotun et al, "The Case for a Single-Chip Multiprocessor", Proceedings of the Seventh International Conference on Architectural

Support for Programming Languages and Operating Systems, Cambridge, MA, Oct. 1996) as applied to claims 1, 4, 14 and 20 above, and further in view of Hassoun (5,737,757).

Arimilli and Olukotun are relied upon for the teachings relative to claims 1, 4, 14 and 20 as above.

The rationale derived from Arimilli and Olukotun in the rejection of claim 13 above is incorporated herein for the teaching that a plurality of processors is linked with the cache via the crossbar interface as in claims 7-10.

The rationale derived from Arimilli and Olukotun in the rejection of claim 3 above is incorporated herein for the teaching that a single address space may be partitioned among two or more caches, and that the crossbar interface comprises a plurality of ports via which a cache and a processor are linked based on the main memory address as in claim 10.

The combination of Arimilli and Olukotun does not teach that the processor is linked with the cache based on an address range stored in the processor corresponding to a range of addresses in the main memory mapped to the cache as required by claim 5.

The combination of Arimilli and Olukotun also does not teach that the processor comprises an address range table wherein each address range is associated with a cache as required by claim 7, and where the table is programmable as required by claim 8.

The combination of Arimilli and Olukotun also does not teach that the processor comprises a plurality of address ranges and module identifiers corresponding to the caches as required by claims 9-10.

The combination of Arimilli and Olukotun also does not teach that a cache and processor are linked based on a module identifier supplied by the processor as required by claims 16-17.

The combination of Arimilli and Olukotun also does not teach that module identifier is associated with a main memory address range in a processor as required by claim 22.

Hassoun teaches a plurality of processors linked to a plurality of memories through a crossbar interface, where the address space of the memory is partitioned into separate address ranges (Fig. 1; column 2, lines 3-5; column 4, lines 20-25). Hassoun further teaches that a transaction initiated by a processor for accessing the memory contains a module identifier of the memory module to which the transaction is sent (Column 4, lines 26-39; column 5, lines 54-63).

It is readily apparent in the foregoing teachings of Hassoun that in order to send the proper identifier of the module associated with the memory address referenced in the transaction, so that the crossbar can direct the transaction to the proper module, the processor must store information to associate the address range mapped to each memory module with the module identifier (i.e. a table).

Regarding claims 5, 7, 9-10, 16-17 and 22, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to apply the teachings of Hassoun regarding directing transactions between a processor and a main memory over a crossbar interface, to the problem of directing transactions between a processor and a cache memory over a crossbar interface in the system of Arimilli and Olukotun, noting that it is well known to interface a cache memory to a processor in place of a main memory in a manner that is transparent to the processor, in order to improve memory access time. Therefore, it would likewise have been obvious to link a processor with a cache based on a main memory address range corresponding to a range of addresses mapped to the cache, where the address range is stored in an address range table in the processor containing a plurality of address ranges such that each address range is associated with a cache, and where each cache is identified by a module identifier, as taught by Hassoun, in the system made obvious by the combination of Arimilli and Olukotun, in order to direct memory transactions to the proper receiving module as taught by Hassoun.

Regarding claim 8, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to make the address range table programmable because it is well known in the art to make configuration data in a system programmable in order to flexibly adapt the system to changing conditions such as the addition, deletion, or failure of components in the system.

8. Claims 11 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli (US 6,532,519) in view of Olukotun (Kunle Olukotun et al, "The Case for a Single-Chip Multiprocessor", Proceedings of the Seventh International Conference on Architectural Support

for Programming Languages and Operating Systems, Cambridge, MA, Oct. 1996) as applied to claims 1 and 14 above, and further in view of Handy (Jim Handy, The Cache Memory Book, 1998).

Arimilli and Olukotun are relied upon for the teachings relative to claims 1 and 14 as above.

The combination of Arimilli and Olukotun does not teach that the system is configured to deliver data from the memory to the cache and the processor at the same time as required by claims 11 and 19.

Handy teaches a cache memory system where upon a read miss, the cache and the requesting processor receive data delivered from a main memory simultaneously so that the new data is available from the cache in the event of a subsequent access to the same data (Page 46, Fig. 2.4b; pages 44-45, paragraph 4).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to deliver data from the memory to the cache and the requesting processor simultaneously as taught by Handy, in the system made obvious by the combination of Arimilli and Olukotun, so that the new data would be available from the cache in the event of a subsequent access to the same data as taught by Handy.

Response to Arguments

9. Applicant's arguments filed 6 April 2004 with respect to the rejections under 35 U.S.C. 102 and 103 contained in the previous office action have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John M Ross whose telephone number is (703) 305-0706. The examiner can normally be reached on M-F 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (703) 306-2903. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mano Padmanabhan 6/10/04

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